Special Session: Hardware design, optimization and system security

The main objective of this session is to provide the platform to the researchers, industry experts, academicians and innovative individuals to get together and discuss the all Emerging trends in IC design technologies along with the optimization related. Further aim is to highlight the importance of security focused hardware design considerations to protect and secure hardware in an efficient manner.

Scope of Interest:
VLSI High performance circuits design, low power design techniques and architecture, IOT enabled circuit design, RF, analog and mixed-signal; Biomedical; Wireline and wireless communication; Digital signal processing (DSP); Memory systems; Reconfigurable and programmable, VLSI algorithms, Performance optimization methodologies, Memory architecture, 3D-IC; Performance modeling, Parasitic modeling, Emerging techniques, FPGA, Artificial Intelligence concepts and their applications in VLSI , Fuzzy and other techniques and their application in VLSI, HW-SW co-design, reconfiguration and debug; System, Design validation and verification, SOC, architecture, routing topologies/networks, NOCs, On-chip interconnect, Identification of new CAD tool feature list, optimization tools., FPGA accelerated computing, IOT enabled FPGA capabilities and applications,

Electronic hardware and systems security , systems security, security aspects in interactions between hardware, systems and firmware, software, security aspects of processor, System-on-Chip (SoC), Field Programmable Gate Arrays (FPGA), PCB, Hardware attacks, vectors, side-channel attacks, piracy, reverse engineering, tampering, and hardware Trojan attacks, security measures at different design stages, architecture definition, design, validation, and deployment. Security and trust considerations for embedded systems, automotive systems, cyber-physical systems, The Internet of Things (IoT), reconfigurable systems, biomedical systems including implants, wearable devices etc

Important Dates:
Paper submission due: September 01, 2019
Notification of paper acceptance: October 15, 2019
Registration and Final manuscript due: October 30, 2019

Chair:
Dr. Manoj Sharma
Associate Professor , Dept. of ECE, Bharati Vidyapeeth's College of Engineering
Paschim Vihar, New Delhi, Aff. G.G.S.I.Univ. Delhi, India
manojs110281@gmail.com