International Journal of Computer Information Systems and Industrial Management Applications.
ISSN 2150-7988 Volume 12 (2020) pp. 310-329

Received: 21 January 2020; Accepted: 01 September, 2020; Published: 28 September, 2020

BARE BOARD MULTILAYER PRINTED CIRCUIT BOARD DEFECT IDENTIFICATION FOLLOWED BY LOCALIZATION

Anitha D B [1] and Dr. Mahesh K Rao[2]

[1] Department of Electronics and Communication Engineering, VVIET
and Research scholar, Maharaja Research Foundation, University of Mysore, India
anithadbvvietec@gmail.com

[2] Department of Electronics and Communication Engineering,
Maharaja Institute of Technology, Mysore, Karnataka, India
maheshkrao_ece@mitmysore.com

Abstract*: In recent years, the Multilayer Printed Circuit Boards are becoming the mainstream of all electronic devices due to its various benefits such as high assembly compactness, small size, and worthy quality. Hence manufacturing of defect-free Multilayer Printed Circuit Board has gained a lot of importance. This paper is mainly focusing on the identification and localization of most commonly occurring defects like Trace Cut, Pad Injury and Trace Short. In this work, a non-contact and referential based algorithm is developed for the inspection of real Multilayer Printed Circuit Boards defects. In this approach, firstly the RGB image of both reference image which is having no defect and Test image will be split in to individual channels of R, G and B. The segmentation process will be applied on individual channels of both reference and test image to obtain the binary images. The comparison of binary images of individual channels is performed to obtain three difference images. The three difference images will indicate Pad Injury, Trace cut and Trace short defects respectively. Once the defects are identified the location of the individual type of defect is obtained by Difference of Gaussian method and maximum filter. Finally, the location of the defect will be highlighted along with label on the test PCB image. The experimentation shows that, the proposed approach successfully performs the inspection of multilayer boards having single defect, multiple similar defect and multiple different defects. Time taken for the inspection of the board is presented and it is ranging from 1627 to 1659 milliseconds depending on the dimension and number of faults. Extensive comparisons of the proposed method with previous methods demonstrate that our proposed approach is more feasible and effective for the inspection of Multilayer PCB for Pad Injury, Trace cut and Trace Short defects.

***Keywords*:** Bare Board Multilayer PCB, Gaussian Difference, Maximum filter, Inspection of Defects.

I. Introduction

Printed circuit boards (PCBs) are very important for all Electronic devices since it provides the basic functions through combinations of components and wiring mechanisms. Single and double layer PCBs are suitable only for simple Electronics devices that have limited functions. Small, lightweight and complex Electronics devices require Multilayer PCBs [1]. Single Layer PCB contains only one copper layer and double-sided PCBs are made up of two copper layers superimposed on one another and the copper layers are bonded together by an insulating layer. Multilayer boards perpetually consist of an even amount of copper layers. A six-layer board constructed by using two double-sided PCBs which makes internal layer couples and every internal layer is developed separately based on the respective artwork and two unprocessed single layer PCBs which makes the outer copper layers. The insulating material will be placed between every layer and the entire layer stack up is bonded together under high temperature and pressure. Now the board looks like double-sided PCB even though it has six layers. Next, the unprocessed outer layers are processed with corresponding artwork which includes track and pad patterns. The two outer layers (Top and Bottom) are known as routing or signal layers which are mainly used for placing the component pads and tracks. Four inner layers are used as power plane, ground plane or routing layer. The power and ground planes are the areas of copper that are connected to either a power supply potential (e.g., VDD) or the ground (0 V) connection [2], [3]. Since separate layers (Inner layers) are used for power and ground more number of components can be placed in multilayer PCB compared to single and double layer PCB. As the quantity of the component rises the difficulty of the board also rises. Based on the customer requirements the PCB Manufacturer develops the multilayer PCB with only Through Hole(TH) components, only Surface Mount(SMT) components or both TH and SMT components. In this paper, the authors used four-layer bare PCB which contains both TH and SMT components pattern for the experimentation. The bare board multilayer PCB mainly contains three features and they are copper trace which is mainly used to connect the various components of the circuit, pads which are the space on the PCB mainly used to place the electronic components, and holes which are mainly used to insert the components.

The key intention to test the final multilayer PCB is to avoid the accumulation of further cost in the production of the

defective product. The cost of the defects is very less if the faults are recognized during the bare board multilayer layer PCB inspection only. The price of the same defect is 10 times more if the defects are identified during the placement of the component. Similarly, the cost of the scrap is increased to 100 times if the faulty assembled PCB used in the system-level. Finally, the cost of scrap or service is increased to 1000 times if the error is found in the field after installation [4].

The Indian Electronics System Design and Manufacturing (ESDM) is one of the fastest growing sectors. As per the report of India Electronics Semiconductor Association (IESA), the demand for electronics in India stood at USD US$45 billion in 2015 and was projected to grow to USD US$400 billion by 2020 and also the market of electronic products in applications such as automobiles, consumer electronics, industrial electronics , IT/ office automation, mobile devices, telecom, medical devices, aerospace & defense and others is sized at $61.8 bn. in 2015 and the sector is expected to reach $123-150 bn. by 2020 [5]. As the PCB industries know that the PCBs are backbone of all these Electronics products, they have to take more precaution during the manufacturing process not only to produce PCB but also to produce the defect free PCB.

In this paper, the set of rules is evolved for the inspection of bare board multilayer PCB images to identify the most typically taking place defects including copper trace cut, trace short and pad injury. According to the analysis of defect Pareto of PCB manufacturing industries 39%, 25%, 18% and 10% of the scraps are because of trace cut, scratch, trace short and pad injury respectively. Left over 08% of the scrap is because of the remaining 26 different types of defects. This paper addressing 67% of the total scrap which is because of Trace cut, Trace short and Pad injury. Initially, the input PCB images are preprocessed using the basic image preprocessing operation. Then the trace and Pad's main features of the PCB images are extracted and processed separately to identify the Trace cut, Trace short and Pad Injury defects. Finally, the information such as size, x and y coordinates of each recognized defects are obtained using Gaussian difference method of blob detection.

The content of the paper is organized as follows: Section II presents the current methods used for the PCB defect detection that motivated the development of the efficient algorithm of the proposed approach. Section III presents the main features or characteristics of the multilayer bare board PCB. Section IV presents the proposed method for extracting the features such as Trace and Pads of the bare board PCB, identifying the PCB defects related to Trace and Pads, extracting features related to location of the identified defect and highlighting the location of the defects on the defected PCB. Next, in Section V the real PCB image data set used for the experimentation and experimental results of multilayer bare board PCB inspection are explained along with the analysis of the obtained result. Finally, conclusions are drawn.

II. Literature Review

The PCB industries are using different techniques to identify the defects in PCB at various stages of manufacturing. The following testing methods are used in the final stage of PCB Inspection

- Flying Probe Test
- Jig Test
- Automatic Visual Inspection
- Manual Inspection

Flying Probe and Jig test are Electrical testing methods that detect only track open and short defects with 100% accuracy. But in these types of testing, the testing equipment directly touches the board and may damage the circuit pattern. The cost of these two types of equipment is around 15 lakhs. Automatic Visual Inspection (AVI) and Manual inspection are Non Electrical testing method which detects all types of defect. These methods do not cause any damage to the board. But these two methods do not result in 100% accuracy of inspection. This machine will perform the inspection of PCB of size 100mmx100mm in 2 seconds. But the cost of AVI machine is around Rs. 1.2crore and it is tough for small scale PCB manufacturing industries to endure such costs [6]. Since all four methods are having their own benefits and drawbacks, the large scale industries are using all four methods to inspect the PCBs and small scale industries are using all the methods except AVI machine in order to increase the correctness of inspection. Obviously the total cost of the inspection, using all four methods will be around Rs. 1.5crores.

The PCB inspection algorithms proposed by various researchers are classified into two categories: the first one is referential approach and the second one is non-referential approach. The referential methods use the complete information of the printed circuit board under test which is commonly known as golden board or reference board. The image comparison and template matching techniques are two examples for referential approach. The non-referential methods use the information of properties common to printed circuit board family. This method does not require the information of particular board under test [7]. In referential method, the identification of printed circuit board features requires more cultured approaches. This approach requires proper alignment. The working of non-referential method is based on some assumption that the features of printed circuit board are geometrical shapes and the unpredicted irregular geometric shapes are considered as defects. The one more task of this method is to identify whether every feature falls inside the necessary dimensions. The precise alignment is not mandatory in this approach. But this approach may result in missing of more number of defects due to distorted features [8]. Various research works were carried out on the following types of bare board PCB images

- Computer generated artificial PCB image
- Computer generated real PCB image
- Natural PCB board image
    - PCB immediately after etching process
    - Final PCB

Initially the researches experimented on artificial computer

generated PCB image which includes the patterns of three varieties of the boards, that is through hole PCB patterns, printed wiring board pattern and surface mount PCB pattern as shown in Figure 1. They compare the good PCB which is not having any defect with the defective PCB which includes all 14 commonly known defects such as open, short, break out, pin hole, over etch, under etch, conductor too close, mouse bite, spur, missing hole, wrong size hole, missing conductor spurious copper and excessive short in order to identify the defects and classify the defects in to number of groups [8].

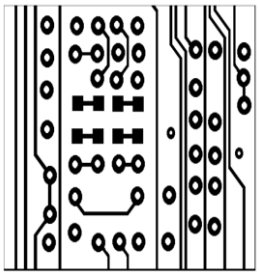


Figure 1. Computer generated artificial PCB image

Prachi et al. proposed an algorithm which detects and classifies all the known 14 types of defects successfully with greater accuracy (70-80%). Defects were detected and classified using image subtraction and KNN classifier [9]. Veena Gaonkar proposed an algorithm to detect and classify 14 known defects in to 13 groups (Short and excess short together).This is done by using morphological segmentation and simple image processing theories. Labeling of the defect was also done on the single layer defective bare PCB [10].

Later, most of researchers worked on the real PCB images of simple hardware circuits generated by the simulation software as shown in Figure 2. In this method, defect detection and classification is based on comparison of defect free simulated PCB image with the defective PCB image. Sanli Tang et al. designed a neural network which perfectly identifies the PCB faults from an input pair of a fault free template and a faulty test image. A novel group pyramid pooling module is proposed to efficiently extract features of a large range of resolutions, which are merged by group to predict PCB defect of corresponding scales. The dataset was generated using simulation software in order to train the deep neural network, which comprises 1,500 image pairs with annotations containing the locations of 6 common kinds of PCB faults such as open, short, mouse bite, spur and copper pin-hole [11]. Jianjie Ma et al. developed an algorithm to discriminate probable fault regions by using a suitable threshold based on the histogram of the difference image. The periphery lengths of the probable fault regions are used to find the real defect. Then the improved region growing method is used to acquire the whole fault region which makes the fault recognition easier. Finally, they recognize every fault such as open, short, spurious copper, spur and mouse bite by determining the changing times of the peripheral boundary pixels' gray scale. The experimentation was conducted on the simulated single layer PCB image and achieved 90% defect detection. But defect recognition rate was only 85% [12].

Can Zhang et al. proposed an algorithm which improves the defect detection in bare PCB by applying the knowledge of deep discriminative features, which intern reduces the large dataset requirement of deep learning method. They used an existing PCB defect dataset with some more artificial defect data and affine transformations to increase the quantity and diversity of defect data. They employed a deep pre-trained convolutional neural network (CNN) to learn high-level discriminative features of defects and fine-tune the base model on the extended dataset by freezing all the convolutional layers and training the top layers. Finally, localize the defect by adopting the sliding window approach. The author addressed only open, short, spur and mouse bite defects in artificially created PCB images [13].

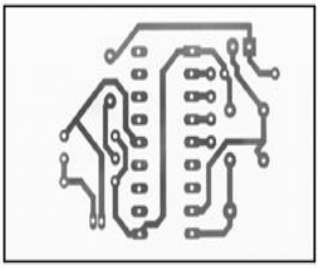
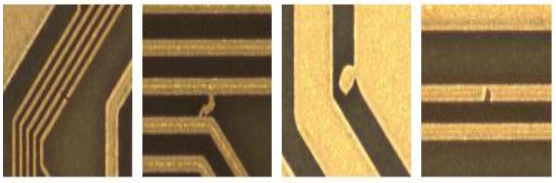


Figure 2. Computer simulated PCB image of real circuit

In the PCB industries, inspection will be carried out at every stage. Among number of stages, two stages are purely depending on the image processing techniques. One is immediately after etching process and the second stage is before packing the final PCB boards which is commonly known as the final inspection process. The portion of the PCB image after etching process is as shown in Figure 3. In recent years, most of researchers have worked on the natural PCB images which are captured from the camera after the etching process of PCB manufacturing.



(a) (b) (c) (d)

Figure 3. PCB image after etching process: (a) Disconnection (b) Connection (c) Projection (d) Crack

Hiroaki Hagi proposed an algorithm to identify the faults present in the PCB captured after etching process of PCB manufacturing process. Firstly, the difference image was obtained by taking the difference between the test image and reference image. Secondly, for each of RGB bands of the difference image binary images are generated. Next, the defect candidate image was obtained by performing the Logical AND of three binary images. Finally, the features related to color and shapes were extracted and used for learning and classification by SVM to recognize both real and pseudo faults. This method may result in misclassification for the class having small number of data. The time taken for the classification was more since the defect candidate region was obtained by the comparison of color reference image with color test image [14]. Harshitha et al. proposed an algorithm for defect detection of natural PCB images captured before the etching process of PCB manufacturing process to inspect

circuit printing which is commonly known as circuit imaging. Angle of tilt is handled using Hough transform and histogram based technique was used for variant height handling and finally the bad light vision condition was taken care using haze removal technique. Bare PCB defects such as pin hole, nick and extra DFPR were identified and sorted for single layer, double layer and multilayer boards. But the experimentation was conducted on the boards having only single defect [15].

Eun Hye Yuk proposed method which detects the defects such as improper etching and scratches in the portion of PCB image captured after etching process of printed circuit board manufacturing. In this paper, features were extracted through speeded-up robust features (SURF), and then calculate the probability by learning the pattern of faults. Next the density of the features was estimated by generating weighted kernel density estimation (WKDE) map weighted by the probabilities. This paper compares the performances of three different methods: Method 1 detects the defected region by observing only the probability found by the random forests based on definite threshold. Method 2 identifies the faults by seeing only the density of the features without considering the probability. Finally, method 3 detects the defects by observing the weighted kernel density estimation value. In this approach both the properties of the features and their density were taken in to account. Authors demonstrated that the method 3 was suitable for identifying a scratch fault on a PCB. They carried out the experimentation on only 10 PCB images having only scratch faults [16].

The final bare board PCB sample obtained after surface finishing and routing is as shown in Figure 4. Only few researchers have worked on the final PCB defect detection.

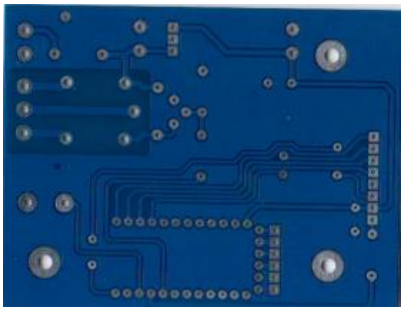


Figure 4. Sample final bare PCB Image

Vikas Chaudhary et al. proposed an algorithm for PCB defect detection and classification. The proposed algorithm is mainly divided into five stages: Registration, pre-processing, segmentation, detection of defect and classification of defect. Depending on the number of connected components the defect classification is performed. They performed the comparison of reference PCB image without having any defect with the test PCB image having all 14 types of defects. They created all the 14 types of defect [8] in the same image and successfully detected and classified the 14 common types of defects. But they have not localized the defect which is the main issue faced by all the PCB fabrication industries [17].

Mehmet Baygin et al. developed fault recognition approach based on the machine vision using image processing to detect only missing hole defect in real PCB Image. They detected the number of holes present in the test PCB and compared the count with that of reference PCB to determine the deficiencies in the holes count. They extracted Y channel and apply Otsu thresholding, canny edge detection and Hough transformation to detect missing holes defect. The algorithm does not depend on the position, direction and color conditions of the PCB. But as per the defect Pareto of bare PCB fabrication industry, the missing hole defect is not belongs to commonly occurring defects in the PCB Industries and accounts for less than 0.1% of total defects [18].

From the literature analysis, it is found that most of the investigators worked on artificially generated single bare board PCB pictures and efficiently detected all known kinds of defects. But only a few researchers worked on defect detection of real single layer PCB images and identified few defects that are not commonly occurring defects in the PCB industries, for example missing hole, wrong size hole etc. The identification and localization of defects in real final multilayer bare PCB is a challenging task. The proposed method will be addressing most commonly occurring defects such as Trace cut, Trace short and Pad Injury in real bare board multilayer PCB image which constitute to about 67% of total defects.

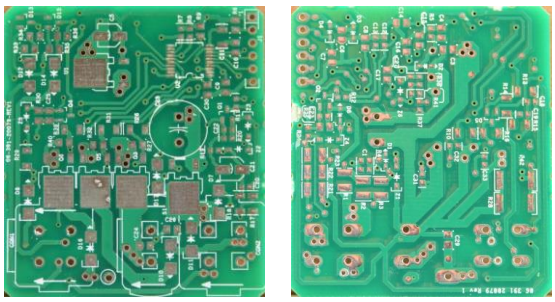
III. Features of Printed Circuit Board

The main input for manufacturing the bare board PCB is the artwork which represents the circuit diagram. It mainly consists of footprint of the component and connecting wires. The footprint or land pattern of the component represents the type, size and number of pins present in that component. The pins of the component are generally called as Pad Stack or Pad. The Pads of through hole component are represented by either circular ring or square ring whereas that of SMT component are represented by either square, rectangular or oval shape pattern. The passive component such as resistor, capacitor and inductor contains only two pad stacks (pin).Whereas, the active components contains various number of pad stacks on only one side, two side or on all four sides based on the component type such as Single in Line Package (SIP), Dual in Line Package (DIP), Quad Flat Package (QFP) or Pin Grid Array (PGA) [1]. Hence the bare board PCB contains only the circuit pattern and this pattern includes connecting wires which are represented by the traces and components land pattern which is represented by set of pads and holes. Obviously the faults in the PCB are related to the Traces, Holes and Pads of PCB. However the PCB fabrication industries are taking enough care to avoid the defects related to holes by using computer programmed CNC machine. The major faults occurring during the manufacturing of bare board PCBs are Trace Cut, Trace short and Pad Damage.

The sample board used for the experimentation of the proposed method is shown in Figure 5 and can be categorized as having SMT pads, Traces and through holes of different size as shown in Figure 6, 7 and 8 respectively using Computer-Aided Manufacture (CAM) software. The sample board contains a number of holes of different sizes as tabulated in Table 1. The total number of through holes present in the sample board is 102. The blue color line in

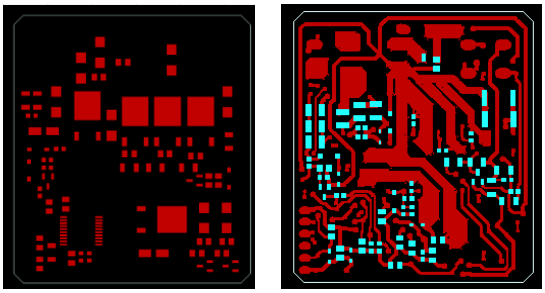
Figure 7 indicates the traces of various widths ranging from 350 micrometer to 2000 micrometer as tabulated in Table 2 and 3. The top layer of the sample board contains number of oval and rectangular shape pads of various size as shown in Figure 6(a) and as presented in Table 4. The total amount of pads present in the top layer of the sample board is 133. The Bottom layer of the sample board contains 105 rectangular shape pads of various sizes as shown in Figure 6(b) and as presented in Table 5. As can be seen there are various parameters to be considered in this image analysis of the PCB, representing a typical PCB.

The details of the sample board discussed in this section indicate that, the bare PCB is mainly characterized by the features such as Trace, Through Hole Pads and SMT Pads. Hence the defects related to these features can be identified by extracting and processing the individual features. This will be explained in detail in the next section.



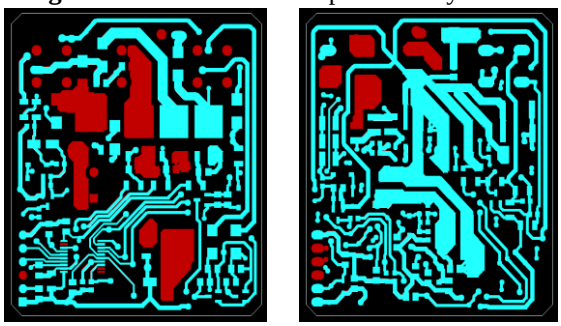
(a)Top Layer (b) Bottom Layer

Figure 5. Sample Multilayer PCB



(a)Top Layer (b) Bottom Layer

Figure 6. SMT Pads of Sample Multilayer PCB



(a)Top Layer (b) Bottom Layer

Figure 7. Traces of Sample Multilayer PCB

Table 1. Through Holes of various size.

Sl. No	Shape	Size in mm	Total No.
1	Circle	0.83	15
2	Circle	1.2	39
3	Circle	6.76	29
4	Circle	7.558	8
5	Circle	9.05	11
Total number of Through Hole Pads			**102**

Table 2. Top layer Traces of Various width.

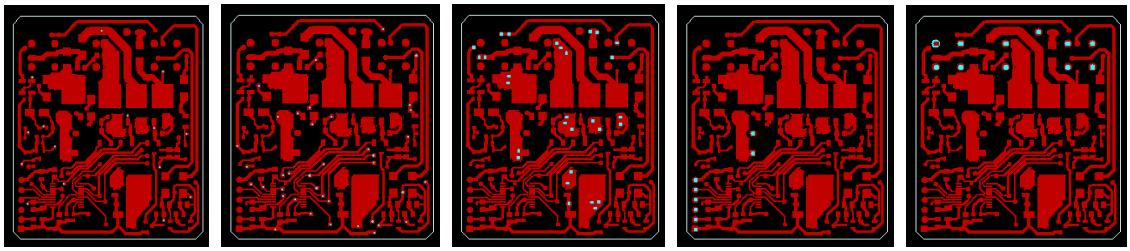
Sl. No	Width of the Track in micro meter	Total No. of Tracks
1	350	62
2	508	213
3	800	131
4	1200	9
5	1500	15
6	2000	7
Total number of Tracks		**437**

Table 3. Bottom layer Traces of Various width

Sl. No	Width of the Track in micro meter	Total No. of Tracks
1	350	9
2	508	283
3	800	257
4	1000	1
5	1100	1
6	1200	5
7	1500	15
8	2000	2
Total number of Tracks		**573**

Table 4. SMT Pads of Various size in Top layer

Sl. No	Shape of the Pad	Size of the Pad in micro meter	Total No.
1	Oval	1501x399	1
2	Rectangular	2649x1651	4
3	Rectangular	5601x6200	4
4	Rectangular	599x1300	3
5	Rectangular	6200x5601	1
6	Rectangular	800x1001	4
7	Rectangular	899x950	8
8	Rectangular	950x899	6
9	Rectangular	1001x800	2
10	Rectangular	1001x1750	6
11	Rectangular	1001x1849	8
12	Rectangular	1151x1450	18
13	Rectangular	1300x599	9
14	Rectangular	1450x1151	14
15	Rectangular	1501x399	19
16	Rectangular	1750x1001	8
17	Rectangular	1849x1001	2
18	Rectangular	2052x2200	16
Total number of SMT Pads			**133**



(a) 0.83mm hole (b) 1.2mm hole (c) 6.76 mm hole (d) 7.558mm hole (e) 9.05mm hole

Figure 8. Through holes of different size for the Sample Multilayer PCB

Table 5. SMT Pads of Various size in Bottom Layer.

Sl. No	Shape of the Pad	Size of the Pad in micro meter	Total No.
1	Rectangular	2664x1262	6
2	Rectangular	564x963	8
3	Rectangular	663x1364	6
4	Rectangular	864x1064	4
5	Rectangular	864x1660	1
6	Rectangular	963x564	2
7	Rectangular	963x1013	16
8	Rectangular	1013x963	18
9	Rectangular	1064x864	2
10	Rectangular	1064x1814	8
11	Rectangular	1214x3366	4
12	Rectangular	1214x1514	6
13	Rectangular	1262x2664	6
14	Rectangular	1514x1214	16
15	Rectangular	1814x1064	2
	Total SMT Pads		**105**

IV. Proposed method

The proposed method mainly focus on the detection and localization of three major types of defect namely Trace cut, Trace short and Pad injury which results in 67% of the total scrap. Figure 9 shows the block diagram of the proposed technique. It has mainly two parts. The first part is defect detection and the second part is defect localization. The Pad Injury, Trace short and Trace Cut defects are identified by processing the R Band, Blue Band along with the grey scale images of reference and test PCB image respectively which is explained in detail in the sub section IV A. The location of the identified defects is extracted using Difference of Gaussian method and maximum filter followed by highlighting the location on the test bare board PCB which is explained in detail in the sub section IV B. The algorithm for PCB defect detection and localization is as depicted in Table 6.

A. Defect Identification

The reference and test PCB images are captured by the camera. The image acquired by the camera includes both foregrounds which contain PCB portion and the background. Hence it is necessary to extract only PCB image from the background. The extracted reference and test PCB images of size MxN are properly aligned using Image registration. The following subsection explains the individual steps of the proposed method as shown in Figure 10 along with the purpose of the respective steps.

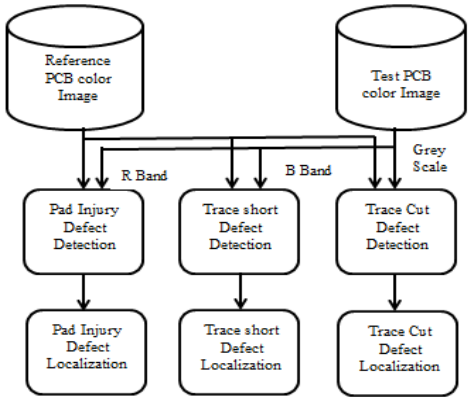


Figure 9. Block diagram of the Proposed method

1) Image resize

In order to process the acquired input PCB image I (x, y) of size M x N within a minimum computational time, it is converted to an image of dimension m x m by resizing the image where m < M and N.

In the manufacturing industry defect identification of the test image should be carried out in real-time i.e., the manufactured PCB when subjected for defect identification it should be processed within a minimum computational time less than 5 seconds. Therefore both the reference and test PCB input images are downscaled to m x m so that, the number of pixels is reduced which in turn reduces the memory storage space and the processing time. As the test and the reference images are both resized exactly the same way, information loss for comparison purpose does not arise.

2) Image splitting

In order to classify the test image, pixel-wise comparison with the reference image is required. The comparison should be such that, the difference between the test image and the reference image should be properly recognized. This requires the features present in the images to be effectively highlighted. Each color image is a combination of three primary color channels; Red, Green, and Blue (RGB). Every channel can be considered as a separate image and each of them carries different information. Hence instead of processing original color image, splitting the RGB into separate channels and processing of individual channel would contribute in highlighting the various features in the image.

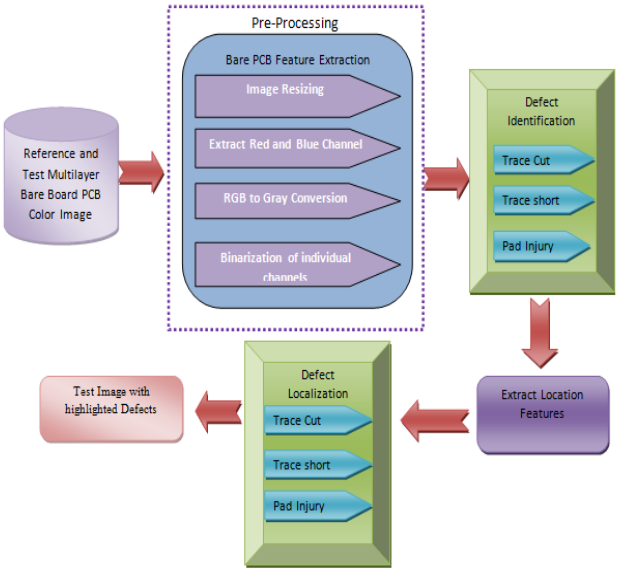


Figure 10. Flow of the proposed method

The given PCB input image consists of background in dark green color, track in light green color and pads in silver color as shown in Figure 5. In the test PCB, if there is a light green color instead of dark green color, then it represents the trace short defects, dark green color instead of light green color represents trace cut defect and also dark green color instead of silver color represents the pad damage defect. Each of these PCB features can be extracted by splitting the input images.

The acquired bare board PCB is RGB image and it has 3 gray scale bands, i.e. red, green, and blue. These gray scale bands are represented by B_R (x, y), B_G (x, y), and B_B (x, y) and they can be expressed by equation 1.

$$Bp(x,y) = 0,1,2,3.....255 \quad p=R,G,B \tag{1}$$

where R, G, B means the gray scale image of red, green, and blue bands respectively, and Bp(x, y) indicates the gray value of the red, green, and blue bands of the RGB image and all of them convey different information. Hence handling of separate bands B_R (x, y), B_G (x, y), and B_B (x, y) would contribute in highlighting the various features in the image [19]-[21].The Pad, one of the main feature of bare PCB and its defect can be obtained by processing of red band image. Similarly the information about the Trace short defects can be identified by processing the blue band Image.

3) RGB to Grey Conversion

The information about trace cut defects can be obtained by processing the grey scale image. Let I(x, y) be the RGB color Image, which is converted into gray scale image using Luma transform

$$I_G(x, y) = B_R(x, y)*0.299 + B_G(x, y)*0.587+B_B(x, y)*0.114 \tag{2}$$

Where I_G(x, y) is the gray scale image, B_R(x, y), B_G(x, y) and B_B(x, y) are the red, green and blue channel of the color image. The information about track and track cut defects can be obtained by processing the grey scale image.

4) Gray to Binary Conversion

The binary image I_B(x, y) is obtained from the gray scale image I_G(x, y) using thresholding method. Binary function I_B(x, y) is defined as

$$I_B(x, y) = \begin{cases} 1 & I_G(x,y) \geq MT \\ 0 & I_G(x,y) < MT \end{cases} \tag{3}$$

Where 1 represents the object feature of the copper traces, 0 represents the background, and MT is a threshold value obtained by taking the mean of gray scale values. The outcome of the conversion is a binary that take only two values, such as white and black [22].

Gray scale Red and Blue channel image are also converted into binary image and they can be used for Pad injury and Trace short defect identification.

5) Inversion of Binary Image

The binary image I_B(x, y) of size m x m is inverted to obtain the inverted binary Image I_{IB}(x, y) using the expression

$$I_{IB}(x, y) = \begin{cases} 1 & I_{B(x,y)=0} \\ 0 & I_{B(x,y)=1} \end{cases} \tag{4}$$

Where x=0, 1, 2.....m-1 and y=0, 1, 2 ...m-1.

Binary Inversion operation will be applied only on binary of gray scale image I_G(x, y) and Red band of the image B_R(x, y).

6) Image Subtraction

Let I_1(x, y) and I_2(x, y) be the two binary input images, then output image I_3(x, y) is received by means of taking the absolute distinction between each pair of corresponding pixels in the two input images.

$$I_3(x,y)= \left| I_1(x,y)-I_2(x,y) \right| \tag{5}$$

The Pad injury defects are found by subtracting the inverted binary of red band test image from that of reference image and it is represented by I_{PJD}(x, y). Similarly inverted binary of gray scale test image is subtracted from that of reference image to identify the trace cut defect which is represented by I_{TCD}(x, y). Whereas Trace short defect is identified by subtracting binary of blue channel test image from that of reference image which is represented by I_{TSD}(x,y).

The difference images obtained in this step indicates the presence of defect in the test PCB. The number of white spot on the black background of the difference image represents the number of defects present in the Test PCB. These difference images can be used as input for the defect localization which will be explained in detail in the next section.

B. *Defect Localization*

The identification of presence of the defect in the PCB is not sufficient. The reason is that, the reworking of the defect present in the PCB is possible only when the testing engineer knows the information about the location of the defect. Hence, here localization of the defect is also taken up as an important research work in consequent to defect identification.

Table 6. Algorithm of the proposed method

PCB Feature extraction and defect detection Algorithm	
1	**Input data :** MI_{Ref} - Multilayer PCB Reference Image, MI_T - Multilayer PCB Test Image of Dimension *MxN*
2	**Intermediate data:** MI_{PDI}- Pad damage Injury, MI_{TCD} -Trace Cut defect, MI_{TSD} -Trace short defect Images
3	**Output data:** $C_X, C_Y, x_1, y_1, x_2, y_2$, MI_{Test}=Test Image with highlighted Pad Injury, Trace Cut and Trace Short defects
4	**Algorithm:**
5	**Begin**
6	Read_RGB_Image (MI_{Ref}, MI_T);
7	Resize MxN dimensioned Reference and Test images to mxm dimensioned images
8	/*Extract R,G,B Channels from the RGB color image */
9	(C_R^{Ref},C_G^{Ref}, C_B^{Ref}) = Extract Bands (MI_{Ref});
10	(C_R^T, C_G^T, C_B^T) = Extract Bands (MI_T);
11	/* Obtain gray scale image from Multilayer PCB Reference and Test RGB Image */
12	(I_G^{Ref}, I_G^T) = RGB2Gray (MI_{Ref}, MI_T) ;
13	/*Obtain the binary form of individual R band, B band and Gray scale image of reference and test PCB image */
14	($C_R^{Ref\_B}$, $C_B^{Ref\_B}$) = Binarization (C_R^{Ref}, C_B^{Ref}) ;
15	($C_R^{T\_B}$, $C_B^{T\_B}$) = Binarization (C_R^T, C_B^T) ;
16	($I_G^{Ref\_B}$, $I_G^{T\_B}$) = Binarization (I_G^{Ref}, I_G^T);
17	/*Obtain the binary inversion of binary R Channel and gray scale image of test and reference image individually */
18	($C_R^{Ref\_BI}$, $C_R^{T\_BI}$) = Invert ($C_R^{Ref\_B}$, $C_R^{T\_B}$);
19	($I_G^{Ref\_BI}$, $I_G^{T\_BI}$) = Invert ($I_G^{Ref\_B}$, $I_G^{T\_B}$);
20	/*Subtract the respective images to identify the Trace cut, Pad Injury, and Trace short defects separately */
21	for k: 0 to n-1 do
22	for m: 0 to n-1 do
23	$MI_{PID} = C_R^{Ref\_BI}(k, m) - C_R^{T\_BI}(k, m)$;
24	$MI_{TCD} = I_G^{Ref\_BI}(k, m) - I_G^{T\_BI}(k, m)$;
25	$MI_{TSD} = C_B^{Ref\_B}(k, m) - B_{T\_bin}(k, m)$;
26	/* Extract the coordinates of the Pad Injury, Trace cut and Trace short defects separately*/
27	$PI_C(CXi, CYi, Ri)$ = Extract_defectscoordinates (MI_{PDD})
28	$TC_C(CXi, CYi, Ri)$ = Extract_defectscoordinates (MI_{TCD})
29	$TS_C(CXi, CYi, Ri)$ = Extract_defectscoordinates (MI_{TSD})
30	/*Find the total number of coordinates */
31	(N_PI_C , N_TC_C , N_TS_C) = Get_totnum_ coordinates (PI_C , TC_C, TS_C)
32	/* Obtain the Marking location of individual type of Defects and highlight it on the test PCB Image*/
33	for j : 1 to *N do*
34	$X1j = CXj - (Rj - \Delta x)$
35	$X2j = CXj + (Rj + \Delta x)$
36	$Y1j = CYj - (Rj - \Delta y)$
37	$Y2j = CYj + (Rj + \Delta y)$
38	I_{Test_M} = Highlight_location ($I_{Test\_M}(X1j, Y1j, X2j, Y2j)$, "label")
39	/* *Repeat step 33-38 for all types of individual defects* */
40	**Stop**

Once the defects are identified, the information about location of the identified defects is extracted by performing the following steps separately on individual difference images $I_{PJD}(x, y)$, $I_{TCD}(x, y)$ and $I_{TSD}(x,y)$ in order to locate pad injury, trace cut and trace short defects respectively

- Obtain two Gaussian blurred images of difference image by performing the convolution of the respective difference image with Gaussian kernel with different standard deviation
- Compute the Difference of Gaussian by subtracting the two blurred images
- Determine the local maxima using Max filter
- Find the peak local maxima's which indicate the position of the defects in terms of coordinates of center point of the defect
- Mark the location of the defect on the test image

The localization of the defect itself takes 91.4% of the total inspection time and for defect detection takes only 8.6% of the total inspection time. Hence the time taken for the localization

of the defects is very high compared to that of defect detection. The following subsection explains the image processing techniques used in the individual steps of the proposed algorithm for defect localization.

1) Gaussian function

The Gaussian function which is also known as Gaussian kernel is mainly used for image blurring. The mathematical expression for this is given by equation 6 [20], [23]

$$G(x.y) = \frac{1}{2\pi\sigma^2} e^{(x^2+y^2)/2\sigma^2} \quad (6)$$

Where x and y are the spatial coordinates of the Gaussian kernel and σ is the standard deviation of the Gaussian kernel. The individual element of the Gaussian kernel or mask can be computed for given value of standard deviation using equation 6.

2) Gaussian Blur

Blurred version of the individual difference image can be obtained by performing the convolution of the difference image $I_D(x, y)$ with the Gaussian kernel G (m, n) by using the equation 7.

$$I^{GB}(m',n') = \sum_x \sum_y G(x,y) I(m' - x, n' - y) \quad (7)$$

The size of the mask is less than the size of the difference image. It is not possible to convolve the entire difference image with mask at a time. The mask is placed on the input image and the convolution is performed between the mask and the input image overlapped with the mask and result is stored in the output location where the center of the mask coincides with the input image. This process has to be repeated till all pixel of the input image is over. In order to get the correct values, one can perform zero padding at the borders of the input image. [20], [23]

3) Difference of Gaussian

For an image, the Difference of Gaussian is obtained by subtracting one Gaussian blurred image of the difference image from the other less blurred image of the same difference image. As discussed in previous section, the Gaussian blurred image is computed form the convolution of the image with the Gaussian kernel. It is computed by the equation 8.

$$DoG_{\sigma_1,\sigma_2}(m,n) = \{ I(m,n) * \frac{1}{2\pi\sigma_1^2} e^{(x^2+y^2)/2\sigma_1^2} - I(m,n) * \frac{1}{2\pi\sigma_2^2} e^{(x^2+y^2)/2\sigma_2^2} \} \quad (8)$$

Gaussian Difference gives zero crossings which represent the edges or areas of pixels that have some variation in their surrounding neighborhood that intern denotes the bright section on dark or dark section on bright in the image $I(m,n)$ which is normally known as blobs [23]-[25]. These edges are called as local maxima's and that are extracted by using the maximum filter which is given by the equation 9.

$$\hat{g}(x,y) = \max\{DoG_{\sigma_1,\sigma_2}(m,n)\} \quad (9)$$

Next, the peak local maxima's are extracted only if the peaks are separated by the minimum distance. In this research work, the minimum distance considered is equal to 1. The coordinates of the peak local maxima's are obtained using Python *skimage.feature.peak_local_max* function. This function returns details of the position of the peak local maxima's such as coordinates of centroid and radius of that region. These coordinates represents the position of the defects present in the Bare Board PCB. In the proposed method, it is possible to obtain the position of multiple defects present in the same board which is not addressed by the previous methods.

4) Marking of Defects

Once the coordinates (c_x, c_y) and radius (r) of the defects are identified, then the top left (x_1, y_1) and bottom right (x_2, y_2) corner of all the defects are obtained by using respective values of c_x, c_y, and r using the equations 10-13.

$$x_1 = c_x - r \quad (10)$$
$$x_2 = c_x + r \quad (11)$$
$$y_1 = c_y - r \quad (12)$$
$$y_2 = c_y + r \quad (13)$$

Finally, the location of the defect $[(x_1, y_1), (x_2, y_2)]$ is marked on the corresponding test PCB. The marking of these location are performed using python Image Library function *PIL.ImageDraw.ImageDraw.rectangle*

V. Results and Discussion

This division exhibits the outcomes of the recommended method used for the detection of bare board PCB defects. The setup and data set used for the experimentation are described in coming sub-sections.

A. Experimental setup

The experimentation of the proposed method for the detection of bare board PCB defects is implemented using the personal computer system with Windows 8 64-bit Operating system, 6 GB installed memory, and Intel core i5 4200U CPU @2.30GHz processor. The software used for the implementation is Python. The camera used in the experiment to capture the PCB image is NIKON D810 which has a resolution of 36.0MP (7360x4912), full frame CMOS sensor of size 35.90mm(h)x24mm(v) and the aspect ratios of 5:4 and 3:2.

B. Description of Dataset

The datasets used for the experimentation are the multilayer bare board PCB images. To evaluate the performance of the proposed algorithm, 200 pieces of PCBs are collected from DMS Technology Pvt. Ltd., Mysuru a Small scale PCB manufacturing industry and inspected by the system developed by the authors.

Table 7. Details of Bare Board Multilayer PCB dataset

Nature of the defect	Number of boards with defects								Total
	Trace cut		Trace short		Pad Injury		Total		
	Top layer	Bottom layer	Top layer	Bottom layer	Top layer	Bottom layer	Top layer	Bottom layer	
Single Defect (SD)	5	6	5	5	27	22	37	33	**70**
Multiple Similar Defect (MSD)	4	4	4	4	6	4	14	12	**26**
Multiple Different Defect (MDD)	Track cut & Track short(TCS)		Track cut & Pad damage(TCP)		Track short & Pad damage(TSP)		Track cut, Track short & Pad damage(TCSP)		**54**
	Top layer	Bottom layer	Top layer	Bottom layer	Top layer	Bottom layer	Top layer	Bottom layer	
	9	5	7	6	8	7	5	7	
Total defective boards									**150**

Among 200 PCB board, 50 are good PCB board and 150 are defective PCB board. Again among 150 boards 80 boards contain the defect in the top layer of the board and 70 boards contains the defects in the bottom layer. The details of the 200 Multilayer bare boards are accumulated from the testing engineer of multilayer bare board fabrication industry who identified the presence of various defects in the board and is as depicted in the Table 7. The board may comprise only one type of defects, more than one similar types of defects or more than one multiple different types of defects.

C. Experimental results

This sub-section delivers the experimental outcomes of the recommended method used for the PCB defect detection. The results in identifying the major three types of bare board PCB defects i.e. Trace cut, Trace short and Pad Injury are demonstrated for top side and bottom side of one board.

Figure 11 shows the experimental results of the proposed method in detecting the PCB Defects. Figures 11(a) and 11(b) are the two input images of the top layer of the multilayer PCB. One is the reference PCB with no defect and the other is the test PCB which has 1 trace cut, 2 trace short and 2 pad damage defects. Totally it contains five defects. In Figure 11 (c)-(g), (h)-(l) and (m)-(q), the individual output of pad damage, track cut and track short defect detection are given respectively. Pad damage defects are detected by processing the R channel of input images. Similarly, trace short and trace cut defects are identified by processing the Blue channel and grey scale images of the input images respectively. Similarly, Figure 12 shows the experimental results for the bottom layer of the multilayer PCB. Figures 12(a) and 12(b) are the two input images. One is the reference PCB with no defect and the other is the test PCB which has 2 trace cut, 2 trace short and 1 pad injury defects. Totally this also contains five defects. In Figure 12 (c)-(g), (h)-(l) and (m)-(q), the individual output of pad injury, trace cut and trace short defect detection are given respectively.

Once the defects are identified, the position of the faults is extracted by Gaussian difference method and the same will be highlighted on the test PCB as shown in Figure 13 and Figure 14. The location of the defect is represented by centroid (X_C, Y_C) and the dimension of the defect (r). The boundary of the defects is represented by [(X_{TL}, Y_{TL}), (X_{BR}, Y_{BR})]. Where (X_{TL}, Y_{TL}) and (X_{BR}, Y_{BR}) are the top left and the bottom right corner of the defect. The information about the location of the defect for every test PCB is tabulated as in Table 8 to Table15.

Table 8, 9, 10 represents the details of the boards having single Trace Cut, Trace Short or Pad Injury Defect on top layer along with coordinates of the defects. The top layer of the sample board contains traces of 6 different widths, more than 5 different trace space, and 23 different size pads. Among 23 pads 5 are circular pads of trough hole devices, one is an oval-shaped pad and 17 are the rectangular shape pad of SMT devices. Similarly, Table 12, 13, 14 represents the details of the boards having single Trace Cut, Trace Short or Pad Injury defect on bottom layer along with coordinates of the defects.

Table 11and 15 represents the details of the boards having multiple similar and multiple different defects along with coordinates of the defects for top and bottom layer respectively. In the case of multiple different defects, the board may contain more than one type of defect. The author performs the inspection of the boards having a maximum of 5 defects of the same type and also of different types. The experiment was conducted on 70, 26, and 54 images with only one type of defect, more than one similar type of defect and more than one different type of defects respectively.

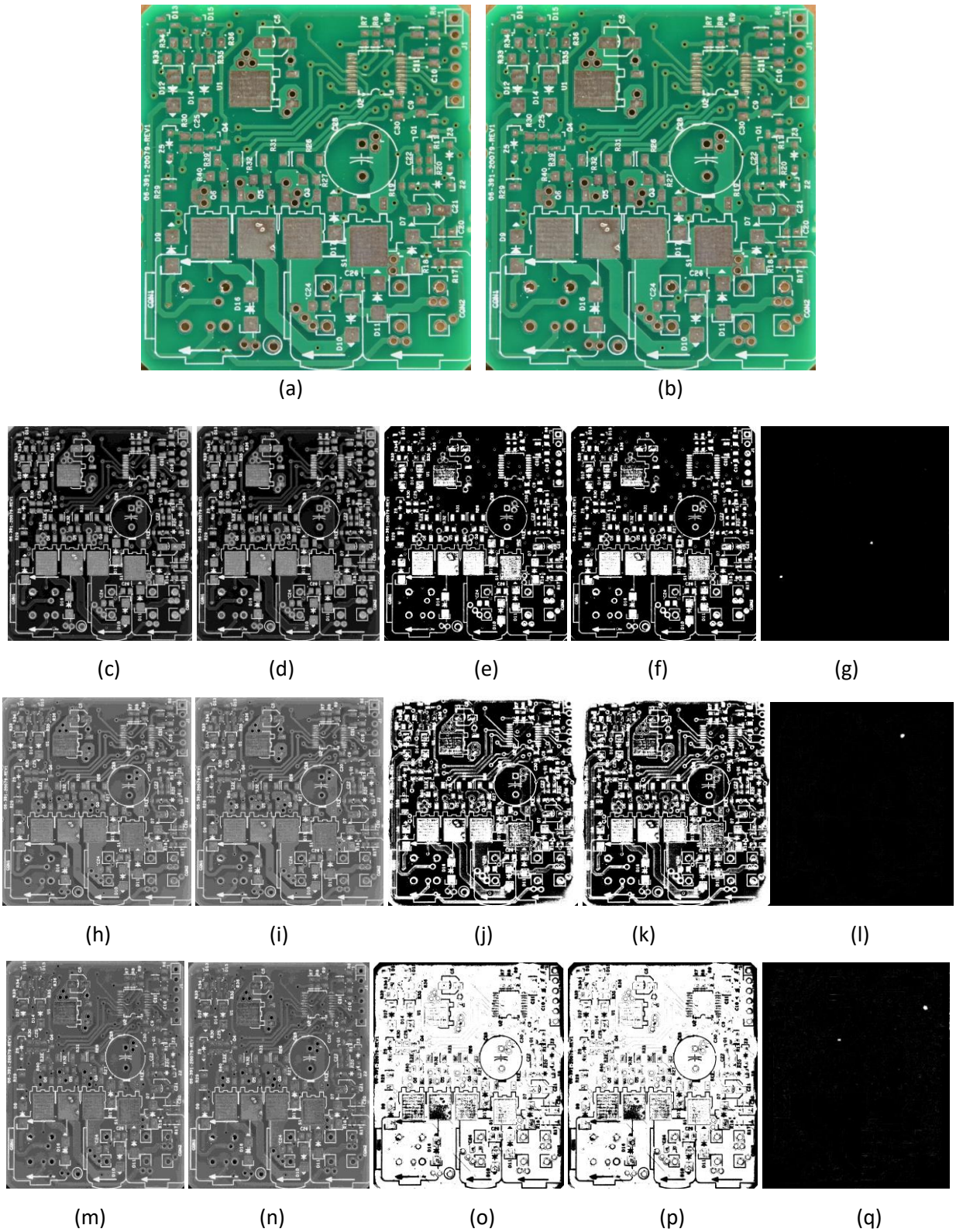


Figure 11. Defect Detection for Top side of PCB - a) Reference multilayer board ,b)Test multilayer board, (c) and (d) are the R band of Reference & Test multilayer board, (e) and (f) are the binary inverted image of R band Reference and Test multilayer board, (g) Pad Injury defect,(h) and (i) are the gray scale image of Reference Test multilayer board,(j) and (k) are the binary inverted image of gray scale Reference and Test multilayer board, (l) Trace Cut defects,(m) and (n) are the blue band of Reference and Test multilayer board,(o) and (p) are binary form of blue band Reference and Test multilayer board, (q) Trace Short defect

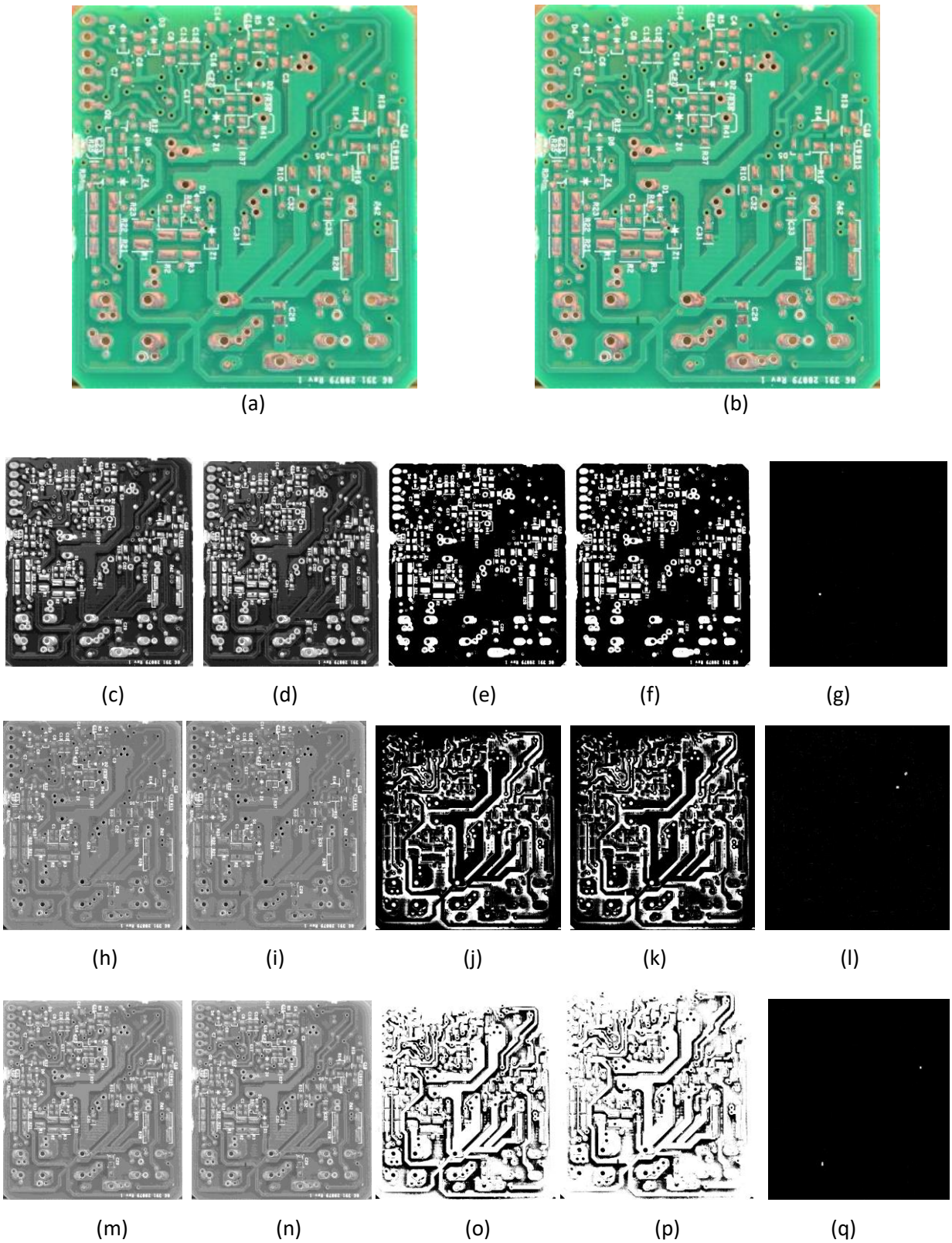


Figure 12. Defect Detection for Bottom side of PCB - a) Reference multilayer board ,b)Test multilayer board, (c) and (d) are the R band of Reference & Test multilayer board, (e) and (f) are the binary inverted image of R band Reference and Test multilayer board, (g) Pad Injury defect,(h) and (i) are the gray scale image of Reference Test multilayer board,(j) and (k) are the binary inverted image of gray scale Reference and Test multilayer board, (l) Trace Cut defects,(m) and (n) are the blue band of Reference and Test multilayer board,(o) and (p) are binary form of blue band Reference and Test multilayer board, (q) Trace Short defect

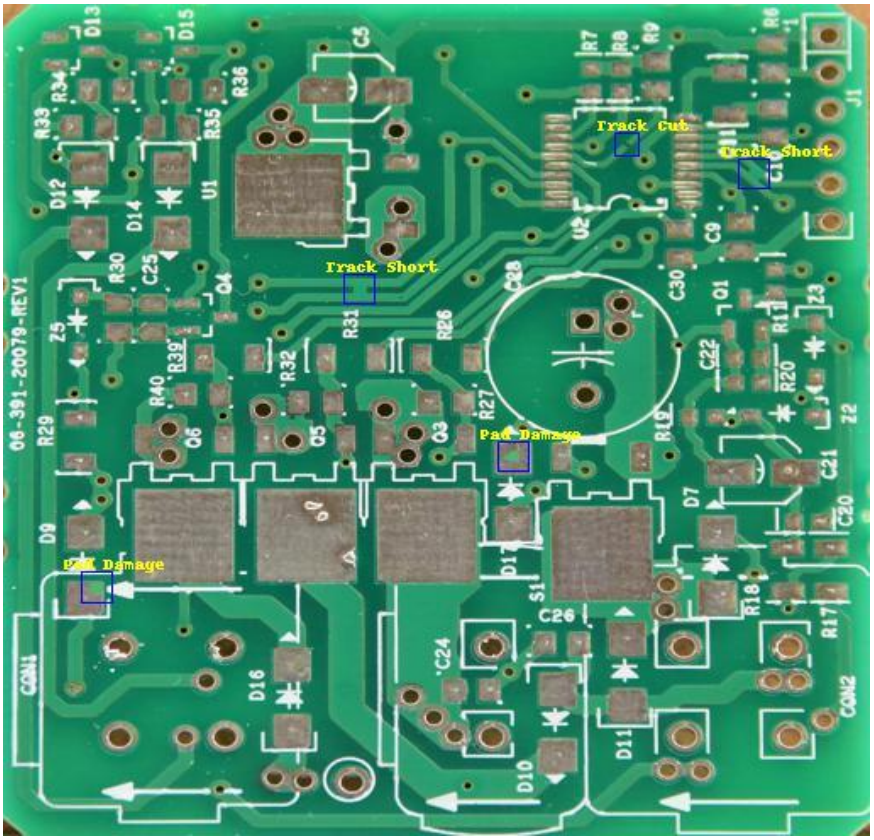


Figure 13. Localization of the defects for Top layer

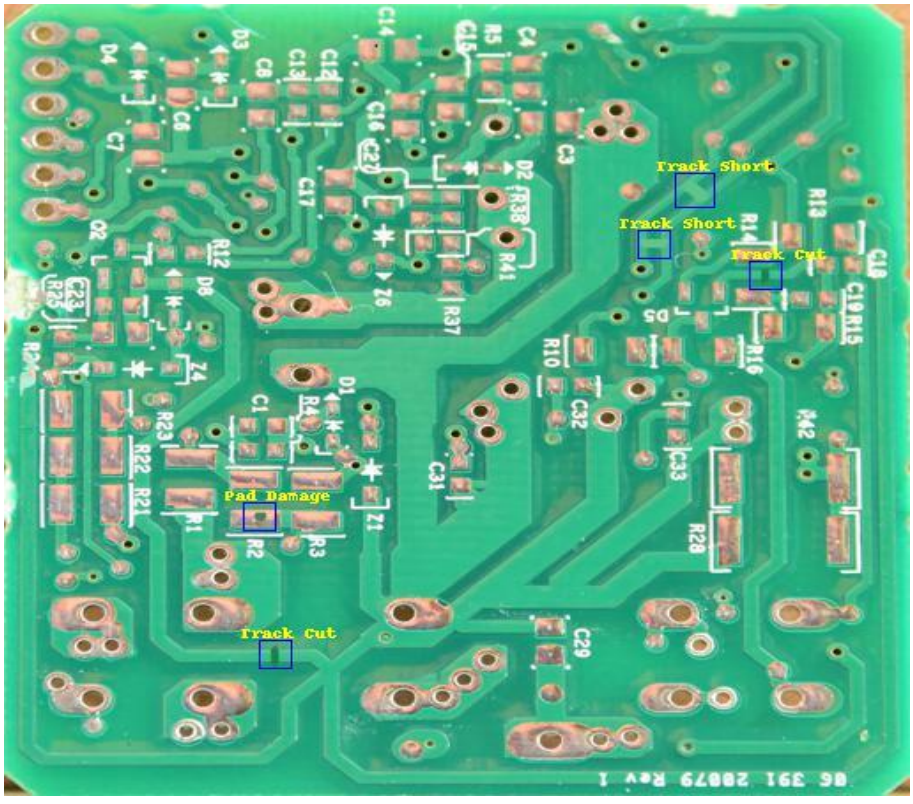


Figure 14. Localization of the defects for Bottom Layer

Table 8. Details of the Board having Single Trace cut Defect on Top Layer

Sl. No.	Track Width in micro meter	Centroid of the Defect		Radii of the defect R	Top left corner of the defects		Bottom right corner of the defect	
		X_c	Y_c		$Y_{TL}= Y_c -r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c -r$	$X_{BR}= X_c - r$
1	350	61	277	3.62	273	57	281	65
2	508	55	324	3.62	320	51	328	59
3	800	110	470	2.262	468	108	472	112
4	1200	375	107	3.62	103	372	111	379
5	1500	416	88	3.62	84	412	92	420

Table 9. Details of the Board having Single Trace short Defect on Top Layer

Sl. No.	Track Space in millimeter	Centroid of the Defect		Radius of the defect R	Top left corner of the defects		Bottom right corner of the defect	
		X_c	Y_c		$Y_{TL}= Y_c -r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c -r$	$X_{BR}= X_c - r$
1	0.2	175	204	3.62	200	171	208	179
2	0.2	155	258	3.62	254	151	262	159
3	0.4	110	271	3.62	267	106	275	114
4	0.4	101	440	3.62	436	97	444	105
5	0.6	187	282	3.62	278	183	286	191

Table 10. Details of the Board having Single pad Injury defect on Top Layer

Sl. No.	Shape and Size of the pad	Coordinate of Center of the defect		Radius of the defect R	Top left corner of the defects		Bottom right corner of the defect	
		X_c	Y_c		$Y_{TL}= Y_c -r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c -r$	$X_{BR}= X_c - r$
1	C7.588R	235	341	5.79	335	229	347	241
2	C6.76R	268	171	3.62	167	258	175	266
3	C9.05R	450	77	3.62	74	447	80	453
4	O1501x399	122	404	3.62	401	197	431	203
5	R501x399	87	326	3.62	323	84	329	90
6	R599x1300	200	428	3.62	425	197	431	203
7	R1300x599	40	62	3.62	59	37	65	43
8	R1700x1001	68	429	3.62	426	65	432	71
9	R1849x1001	97	233	3.62	230	94	236	100
10	R1001x1849	265	274	5.79	268	259	280	271
11	R1151x1450	53	106	3.62	103	50	109	56
12	R1450x1151	184	67	3.62	64	181	70	187
13	R950x899	197	480	3.62	477	194	483	200
14	R899x950	53	348	3.62	345	50	351	56
15	R800x1001	213	45	3.62	42	210	48	216
16	R1001x800	254	404	3.62	401	251	407	257
17	R1001x750	163	456	3.62	453	160	459	166
18	R2649x1651	53	189	3.62	185	49	193	57
19	R5601x6200	315	104	5.79	98	309	110	321
20	R6200x5601	105	176	5.79	170	99	182	111
21	R2052x2200	359	55	3.62	52	356	58	402

D. Performance Analysis

The performance of the proposed method in detecting the defects present in bare board multilayer PCB images is illustrated in this section. The analysis performed based on the size, type, and a quantity of defects present in the board and time taken for the detection and localization of the defects.

Initially, the reference multilayer bare board PCB image will be read and preprocessed and kept in memory. This process will be carried out only one-time because the testing happens by comparing all the test boards with the same reference PCB board. The amount of time required for this will be around102.32msec.

The time taken for the individual process of the suggested method for the examination of multilayer bare board is depicted in Table 16. As the dimension of the fault rises, the time required for the examination of the multilayer bare board having a single defect also increases as shown in Figure 15. Similarly, as the quantity of faults rises, the time required for the examination also increases as shown in Figure16. Based on the overall quantity of faults present in the board and dimension of different faults, the time taken by the proposed method is ranging from 1627msec to 1660msec.

Table 11. Details of the Board having Multiple Defects on Top layer

Sl. No.	Nature-Number of Defects	Type of Defect	Centroid of the defect		Radii (r)	Top left corner of the defects		Bottom right corner of the defect	
			X_c	Y_c		$Y_{TL}= Y_c - r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c + r$	$X_{BR}= X_c + r$
1	MSD - 2	Track cuts	134	125	3.62	121	131	129	138
			55	324	3.62	320	51	328	59
2	MSD -4	Track shorts	104	443	3.62	439	100	447	108
			400	33	3.62	29	396	37	404
			81	378	1.41	376	79	380	83
			187	282	3.62	278	183	286	191
3	MSD -5	Track shorts	104	443	3.62	439	100	447	108
			400	33	3.62	29	396	37	404
			81	378	1.41	376	79	380	83
			187	282	3.62	278	183	286	191
			156	28	5.79	22	150	34	162
4	MSD -2	Pad Damages	359	55	3.62	51	355	59	363
			278	301	3.62	297	274	305	282
5	MDD -2 (TCS11)	Track cut-1	77	359	3.62	354	73	363	81
		Track short-1	175	204	3.62	200	171	208	179
6	MDD -3 (TCP12)	Track cut-1	171	211	2.26	209	169	213	173
		Pad Damages-2	359	55	3.62	51	355	59	363
			278	301	3.62	297	274	305	282
7	MDD -4 (TSP13)	Track short-1	87	299	3.62	295	83	233	91
		Pad Damages-3	359	55	3.62	51	355	59	363
			278	301	3.62	297	274	305	282
			52	104	3.62	100	48	108	56
8	MDD -5 (TCSP122)	Track cut-1	86	368	2.26	366	84	370	88
		Track short-2	175	210	3.62	206	171	214	179
			104	443	3.62	439	100	447	108
		Pad Damages-2	359	55	3.62	51	355	59	363
			278	301	3.62	297	274	305	282

Table 12. Details of the Board having Single Trace cut Defect on Bottom layer

Sl. No.	Track Width in micrometer	Coordinate of Center of the defect		Radii of the defect	Top left corner of the defects		Bottom right corner of the defect	
		X_c	Y_c	r	$Y_{TL}= Y_c - r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c - r$	$X_{BR}= X_c - r$
1	350	115	94	3.62	90	111	95	119
2	508	227	129	5.79	123	221	135	233
3	800	379	86	5.79	80	373	92	385
4	508	451	184	5.79	178	445	190	457
5	800	126	396	3.62	392	122	400	130
6	350	309	47	2.26	45	307	49	311

Table 13. Details of the Board having Single Trace short Defect on Bottom layer

Sl. No.	Track Space in millimeter	Coordinate of Center of the defect		Radii of the defect	Top left corner of the defects		Bottom right corner of the defect	
		X_c	Y_c	r	$Y_{TL}= Y_c - r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c - r$	$X_{BR}= X_c - r$
1	0.2	155	367	3.62	363	151	371	159
2	0.4	163	144	5.79	138	157	150	169
3	0.4	111	400	5.79	394	105	406	117
4	0.4	140	169	3.62	165	136	173	144
5	0.6	78	420	5.79	414	72	426	84

E. Inspection Accuracy

At the period of testing, 200 number of multilayer bare board PCB are inspected. Each board has two sides i.e. component side and solder side. Among 200 PCB boards, 50 are good and 150 are defective. Again in 150 boards, 80 boards contain defects only in the component side and the other 70 boards contain defects only in the solder side. So, totally there are 250 non defective images and 150 defective images.

With reference to the Table 7, these 150 defective images are categorized as (1) Images with only one defect; (2) Images with multiple similar defects; and (3) Images with multiple different defects.

Table 14. Details of the Board having Single Pad Injury defect on Bottom layer

Sl. No.	Shape and Size of the pad	Coordinate of Center of the defect		Radii of the defect R	Top left corner of the defects		Bottom right corner of the defect	
		X_c	Y_c		$Y_{TL}= Y_c - r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c - r$	$X_{BR}= X_c - r$
1	R2664x1262	294	107	2.26	105	292	109	296
2	R1262x2664	287	33	2.26	31	285	35	289
3	R1214x3366	305	410	3.62	406	301	416	309
4	R963x1013	272	138	2.26	136	270	140	274
5	R1064x1814	208	464	2.26	462	206	466	210
6	R1814x1064	189	424	2.26	422	187	426	189
7	R1514x1214	402	312	2.26	310	400	314	404
8	R1214x1514	29	226	2.26	224	27	228	31
9	R1013x963	316	207	2.26	205	314	209	318
10	R1064x864	106	276	2.26	274	104	278	108
11	R663x1364	177	55	2.26	53	175	55	179
12	R564x963	282	186	2.26	184	280	188	284
13	R963x564	235	94	2.26	92	232	96	237
14	R864x1064	205	394	2.26	392	203	396	207
15	R864x1660	410	789	5.79	393	203	397	207
16	C7.588R	395	241	5.79	235	389	247	401
17	C6.76R	395	462	5.79	456	389	468	401
18	C9.05R	394	130	5.79	124	388	136	400

Table 15. Details of the Board having Multiple Defects on Bottom layer

Sl. No.	Nature-Number of Defects	Type of Defect	Coordinate of Center of the defect		Radii of the defect r	Top left corner of the defects		Bottom right corner of the defect	
			X_c	Y_c		$Y_{TL}= Y_c - r$	$X_{TL}= X_c - r$	$Y_{BR}= Y_c - r$	$X_{BR}= X_c - r$
1	MSD - 2	Track cuts	454	185	5.79	179	448	191	450
			421	146	3.62	142	417	150	425
3	MSD -3	Track shorts	341	336	3.62	332	337	340	345
			155	367	3.62	363	151	371	159
			120	390	5.79	384	114	396	126
4	MSD -4	Pad Damages	194	179	2.26	177	192	181	196
			54	166	2.26	164	52	168	56
			332	134	3.62	130	328	138	336
			99	80	2.26	78	97	82	101
5	MSD -5	Pad Damages	203	394	3.62	390	199	398	207
			194	179	2.26	177	192	181	196
			54	166	2.26	164	52	168	56
			332	134	3.62	130	328	138	336
			99	80	2.26	78	97	82	101
6	MDD -2 (TCS11)	Track cut-1	421	139	3.62	135	417	143	425
		Track short-1	78	420	5.79	414	72	426	84
7	MDD -3 (TCP12)	Track cut-1	227	129	5.79	123	221	135	233
		Pad Damage-2	194	180	2.26	178	192	182	196
			58	101	2.26	99	56	103	60
8	MDD -4 (TCS22)	Track cuts-2	420	153	3.62	149	416	157	424
			175	430	3.62	426	171	434	179
		Track shorts-2	155	367	3.62	363	151	137	159
			120	390	5.79	384	114	396	126
9	MDD -5 (TCSP221)	Track cuts-2	420	153	3.62	149	416	157	424
			175	430	3.62	426	171	434	179
		Track shorts-2	155	367	3.62	363	151	371	159
			120	390	5.79	384	114	396	126
		Pad Damage-1	331	144	3.62	140	327	148	335

Table 16. Time taken for individual process

Sl. No.	Operation	Time taken in msec.
1	Reference Image read & preprocessing (one time process)	102.32
2	Test Image read and preprocessing	102.32
3	Track cut defect recognition & localization	508.36
4	Track short defect recognition & localization	508.36
5	Pad damage defect recognition & localization	508.36
Total time including one time process		**1729.72**
Total time excluding onetime process		**1627.40**

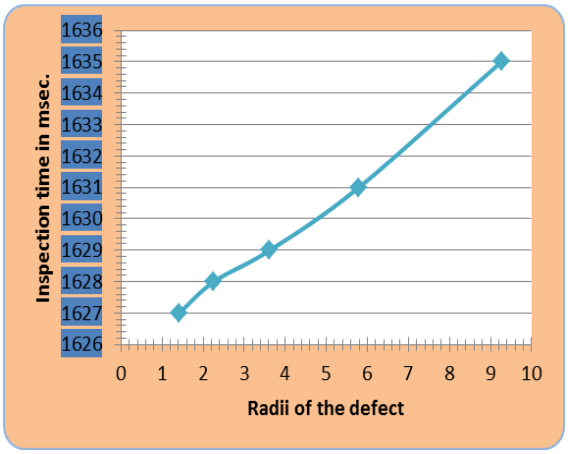


Figure 15. Time taken for the inspection of the board having only one fault with varying radii

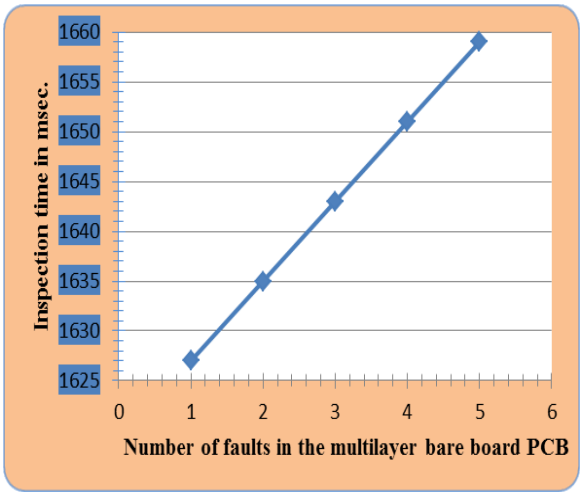


Figure 16. Time taken for the inspection board with variation in quantity of faults

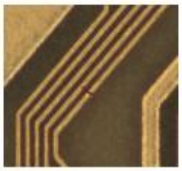
The author successfully inspected 393 images out of 400 images and results in accuracy of 98.25%. For the remaining seven images algorithm fails to compute the position of some track short or pad damage defects because the size of the defects present in these boards is less than 9 pixels. In terms of The experimentation was conducted on single layer PCB image which is captured after the etching process of PCB the number of defects, the author inspected a totally of 371 defects by putting together all 150 defective images. Among 371 defects, 159 are pad damage, 106 are track cut and 106 are track short defects. Accuracy of the inspection of these three defects is as represented in Table 17. The inspection fails only when the radii of the defect is less than 1 or the size of the defect is less than 3x3 pixels in the scale downed input image.

Table 17. Inspection Accuracy of the proposed method

Name of the Defect	Total Number of defects	Number of defects detected	Accuracy of detection
Pad Damage	159	153	96.22%
Track Cut	106	106	100%
Track Short	106	105	99.05%
All	**371**	**364**	**98.11 %**

Table 18 shows that the proposed approach has high accuracy of inspection compared with the previous approaches. Jianjie compares the target image with the standard image to obtain the difference image and then identify the regions of the various defects such as short, open, mouse bite and spurious copper by analyzing the histogram of the difference image.

Table 18. Comparative Analysis

Author	Nature of Input PCB	Printed Circuit Board Image	Accuracy of Inspection
Hiroaki [14]	Single Layer PCB after the Etching Process		93.38%
Jianjie [12]	Single Layer PCB after Etching Process		90.08%
Proposed System	Final real Multilayer Bare PCB		98.11%

manufacturing and got 90.08% accuracy of inspection [12]. Hiroaki Hagi was also conducted the experiment on same type

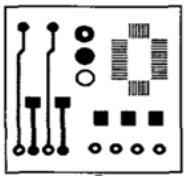
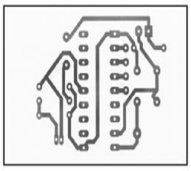
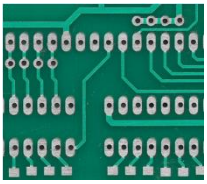
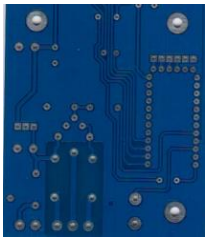
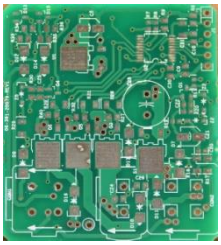
of PCB image and got 93.38% of accuracy for defect classification [14]. But the proposed method is experimented on complex Multilayer PCB and results in 98.18% of inspection accuracy. This method performs defect detection, classification, and localization along with labeling of the corresponding defect type. Thus this method seems to be better suited.

F. Comparative Analysis

This section gives a comparison of this method with other existing approaches which conducts the experimentation on real final PCB images based on the complexity of the input board and inspection time.

Z Ibrahim used a 400x400 synthetic image pattern of printed circuit board which comprises only 4 traces, 6 surface mount pads and 13 TH pads for the experimentation and successfully classified 14 common types of defects in to six groups [26].

Table 19. Comparison of proposed method with several other approaches

Sl. No.	Author	Dimension of the Image	Variety of the Printed Circuit Board	Printed Circuit Board Image	Inspection Time in terms of sec
1	Z. Ibrabim [26]	400 x 400	Synthetically created Printed Circuit Board image outline which comprises 4 trace, 6 Surface mount pads and 13 TH pads		4.7
2	Ismail Ibrahim [27	917x1580	Computer-generated Real PCB Layout		28.8
3	Vikas Chaudhary [17]	1872x1424	Computer generated single layer PCB (24 tracks 10 SMT pads and 46 TH pads		2.5
4	Mehmet Baygin [18]	1270x720	Final real Bare Board PCB (24 tracks and 90 Through holes		7.3
5	Proposed System	2305x2553	Final real Multilayer PCB (437 tracks, 133 SMT pads and 105 TH pads)		1.6

Ismail Ibrahim used a 917x1580 printed circuit board Image which was produced by the simulation tool and this image comprises nearly 18 traces and 30 holes for the experimentation and performed only defect detection and

classification [27]. Vikas Chaudhary performed the experiment on single layer PCB which contains only 24 traces, 10 SMT pads and 46 TH pads. Successfully detected and classified the 14 common types of defects. The time taken for the inspection was around 2.5 sec compared to our method of less than 1.7sec with localization on more complex board. But they have not localized the defect which is the main issue faced by all the PCB fabrication industries [17].

Mehmet Baygin conducted the experimentation on simple real double layer bare PCB which includes only 24 traces, 90 through hole pads and zero surface mount pads. They concentrated only on the identification of missing holes. But this method does not provide any information about the location of missing hole. Also this missing hole defect is not belongs to commonly occurring defects in the PCB industries and it accounts for less than 0.1% of total defects [18]

The proposed technique used the real multilayer PCB which is actually used in high end electronic systems. The experimentation is carried out on 200 multilayer bare PCB. The component side of the board contains around 437 traces, 133 surface mount pads, 105 through-hole pads. Whereas the solder side of the board contains around 573 traces, 105 surface mount pads, and 105 through-hole pads. The time taken for the experimentation is around 1.6 sec.

From this comparison, it can be noticed that the input board used in the experimentation of the proposed method is very complex and large size which contains more number of Traces, SMT pads and Though hole pads compared to the printed circuit board used by other authors. This method performs defect detection, classification and localization along with labeling of type of the defect for the final Multilayer PCB which includes single, multiple similar or multiple different types of defects. Also, the time taken for testing the PCB by the proposed technique is very less compared to all other earlier approaches as depicted in Table 19. The proposed technique can be used in the multilayer PCB fabrication industries to perform the final inspection.

VI. CONCLUSION

This paper predominantly focuses on the inspection of PCB to identify the faults which leads to major scrap during the manufacturing process of PCB. The main idea of the suggested process is to identify and localize the defects related to traces, surface mount and through-hole pads of multilayer PCB by comparing the extracted R band, B band, and gray scale image of color test PCB image with the that of color reference PCB image. At present the large scale PCB industries perform the inspection of final PCB by using automatic visual inspection machine and this device will performs the inspection of PCB of size 100mmx100mm in 2 seconds. This machine shows only the location of the defect and not gives any information about the type of defect. As mentioned in the earlier section, the cost of this machine is around 1.2crore. Even today, the small scale industries perform the inspection of the final PCB by the manual process under illuminating magnifiers which is very tedious, time-consuming and less accurate. Hence the proposed method whose cost is around 2 lakhs and which performs the inspection of PCB of size 90mmx80mm within a time of 1.63 seconds with 98 % accuracy will definitely help the small scale industries to perform the final inspection of the PCBs.

In the future, authors are going to develop techniques for identification of other multilayer PCB defects such as scratch, void, smear etc.

Acknowledgment

This research work is technically supported by the small scale PCB fabrication industry “DMS Technologies Pvt. Ltd.”, Mysore, Karnataka, India. Authors wish to acknowledge the MRF for the support of this research.

References

[1] R Kandhapur, "Printed Circuit Boards Design, Fabrication, and Assembly ", McGraw- HILL Electronic Engineering, 2005.

[2] Hanqiao Zhang, Steven Krooswyk and Jeff Ou , “High Speed Digital Design: Design of High Speed Interconnects and Signaling”, MORGAN KAUFMANN publisher, an Imprint of Elsevier ,2015

[3] Anitha D B and Mahesh Rao, "A Survey on Defect Detection in Bare PCB and Assembled PCB using Image Processing Techniques", IEEE International conference WiSPNET2017, March 2017, pp. 39-43

[4] Clyde F.Coombs,Jr., "Printed Circuits Handbook" , Sixth Edition, McGRAW-HILL, 2008.

[5] Indian ESDM Industry update, An IESA EY Report Executive Summary February 2017

[6] Peter Edelstein, Teradyne, "Comparing costs and ROI of AOI and AXI", North Reading, Massachusetts, USA August 7, 2013

[7] Anoop K. P, Sarath N.S, Sasi Kumar V. V, “A Review of PCB Defect Detection Using Image Processing”, International Journal of Engineering and Innovative Technology (IJEIT) Volume 4, Issue 11, May 2015

[8] Madhav Moganti, Fikret Ercal, Cihan H. Dagli and Shou Tsunekawa, “Automatic PCB Inspection Algorithms: A Survey”, Computer vision and Image understanding, Volume 63, Issue2, March 1996, Pages 287-313.

[9] Prachi P. Londe and S. A. Chavan, “Automatic PCB Defects Detection and Classification using Matlab,” International Journal of Current Engineering and Technology, June 2014, Vol.4.

[10] Veena Gaonkar, “PCB Defect Inspection System using Mathematical Morphology and MATLAB Image Processing Tools,” International Journal for Research in Technological Studies, Vol. 2, Issue 2, January 2015.

[11] Sanli Tang, Fan He, Xiaolin Huang, Jie Yang,” ONLINE PCB DEFECT DETECTOR ON A NEW PCB DEFECT DATASET” arXiv:1902.06197v1 [cs.CV] 17 Feb 2019

[12] Jianjie Ma,” Defect Detection and Recognition of Bare PCB Based on Computer Vision”, Proceedings of the 36th Chinese Control Conference July 26-28, 2017, ISSN: 1934-1768, Dalian, China

[13] C. Zhang, W. Shi, X. Li, H. Zhang and H. Liu, "Improved bare PCB defect detection approach based on deep feature learning," The Journal of Engineering, vol. 16, pp. 1415-1420, 2018

[14] Hiroaki Hagia , Yuji Iwahoria , Shinji Fukuib, Yoshinori Adachia , M. K. Bhuyanc,” Defect classification of electronic circuit board using SVM based on random

sampling", 18th International Conference on Knowledge-Based and Intelligent Information & Engineering Systems - KES2014, Published by Elsevier, Pages 1210-1218.

[15] Harshitha and Dr.Mahesh Rao, " PCB defect detection and sorting using image processing techniques," International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE) Vol. 3, Issue 5, May 2016

[16] H. Y. Eun, H. P. Seung, P. Cheong-Sool and B. Jun-Geol, "Feature Learning-Based Printed Circuit Board Inspection via Speeded-Up Robust Features and Random Forest," Applied Sciences, vol. 8, no.6, 2018.

[17] Vikas Chaudhary, Ishan R. Dave and Kishor P. Upla," Automatic Visual Inspection of Printed Circuit Board for Defect Detection and Classification" IEEE International Conference on Wireless Communications, Signal Processing and Networking WiSPNET 2017,Pages 752-757.

[18] Mehmet Baygin , Mehmet Karakose, Alisan Sarimaden,and Erhan Akin, "Machine Vision based Defect Detection Approach using Image Processing", IEEE conference on International Artificial Intelligence and Data Processing Symposium (IDAP), 2017, 978-1-5386-1880-6/17/$31.00 ©2017 IEEE

[19] Adrien Depeursinge, Omar S. Al-Kadi, J.Ross Mitchell, "Biomedical Texture Analysis: Fundamentals, Tools and Challenges", Academic Press, an imprint of Elsevier, 2018.

[20] Rafael C. Gonzalez, Richard E Woods, "Digital Image Processing", LPE, Third Edition, 2009.

[21] Jan Erik Solem , "Programming Computer Vision with Python", O'Reilly Media, Inc., 2012.

[22] C. A. Glasbey, "An analysis of histogram-based thresholding algorithms", CVGIP: Graphical Models and Image Processing, vol. 55, pp. 532-537, 1993.DOI:10.1006/chip.1993.1040.

[23] Robert A. Schowengerdt, "Remote Sensing Model and methods for Image Processing", 3rd edition, 2007

[24] T. Lindeberg "Image matching using generalized scale-space interest points", Journal of Mathematical Imaging and Vision, volume 52, number 1, pages 3-36, 2015

[25] T. Lindeberg "Scale invariant feature transform", Scholarpedia, Journal of Mathematical Imaging and Vision volume 46, pages177–210, 2013

[26] S.H. Indera Putera and Z. Ibrahim, "Printed Circuit Board Defect Detection Using Mathematical Morphology and MATLAB Image Processing Tools", 2010, 2nd International Conference on Education Technology and Computer (ICETC).

[27] Ismail Ibrahim, Zuwairie Ibrahim, Kamal Khalil, Musa Mohd Mokji, Syed Abdul Rahman Syed Abu Bakar, Norrima Mokhtar and Wan Khairunizam Wan Ahmad, "An Improved Defect Classification Algorithm for Six Printing Defects And Its Implementation On Real Printed Circuit Board Images", International Journal of Innovative Computing, Information and Control Vol. 8, no. 5(A), May 2012.

Author Biographies

Anitha D B is associate Professor on Electronics and Communication Engineering at Vidya Vikas Institute of Engineering and Technology, Mysor, India. She is currently pursuing PhD at Maharaja Research Foundation, Mysore recognized by University of Mysore, India. Her current research interest includes Signal and Image Processing.

Mahesh K Rao is full Professor on Electronics and Communication at Maharaja Institute of Technology, Mysore, and Karnataka, India. He has completed his B.E in E&C from university of Mysore, Karnataka, India. He has done M.A.Sc from university of Windsor, Ontario, Canada. He has completed his PhD from University of Wyorning, Laramine, USA in 1988. He has vast experience working in Industry, as an Enterpruner and as an educator. His research interest includes wireless Sensor Networks, Image and video Processing.